IN THE CLAIMS

Amend claims 13-15, 22 and 32 as follows.

1. (Previously Presented) A data processor comprising:

a CPU for outputting a first address;

address translation means for inputting said first address, translating said first address to a second address, and outputting said second address; and

address output means for inputting said second address and outputting said second address to an external device,

wherein said address translation means stores an external device control information for controlling said external device in association with at least either one of said first address or said second address, and outputs said external device control information to said external device via said address outputting means,

wherein said external device control information is an information which specifies at least one of an access timing, a memory attribute, and a bus width of said device.

2. (Previously Presented) A data processor according to claim 1, wherein said external device is a device having a PCMCIA interface, and said external device control information

is an information which specifies at least one of an access timing, a memory attribute, and a bus width of said device having a PCMCIA interface.

3. (Original) A data processor according to claim 2, wherein said address output means has a timing controller and a bus width and memory attribute decider.

4. (Previously Presented) A data processor according to claim 2, wherein said CPU, said address translation means, said address output means, and said PCMCIA interface in said external device are formed on the same semiconductor substrate.

5. (Previously Presented) A data processor according to claim 1, wherein said second address outputted from said address output means is inputted to said address output means via a cache memory and a bus.

6. (Previously Presented) A data processor according to claim 1, wherein the control information except for an address is not included in said first address.

7. (Previously Presented) A data processing system comprising:

a first address for being outputted by a CPU;

address translation means for translating said first address to a second address; and

address output means for outputting an address to both a first external device and a second external device,

wherein when said first address is outputted to said first external device via said address output means, said address output means outputs first external device control information stored in said address output means in association with said first address, together with said first address to said first external device and

when said second address is outputted to said second external device via said address output means, said address output means outputs second external device control information stored in said address translation means in association with either said first address or said second address, together with said second address to said second external device,

wherein said external device control information is an information which specifies at least one of an access timing, a memory attribute, and a bus width of said device.

8. (Original) A data processing system according to claim 7, wherein said second external device is a device having a PCMCIA interface.

9. (Canceled).

10. (Previously Presented) A data processing system according to claim 8, wherein said address translation means outputs said second address; and

said second address is inputted to said address output means via a cache memory and a bus.

11. (Previously Presented) A data processing system according to claim 8, wherein said second external device has a memory or a modem, and said memory or said modem are controlled by said PCMCIA interface controlled by said second external device control information.

12. (Previously Presented) A data processing system according to claim 8, wherein said CPU, said address translation means, said address output means, and a PCMCIA interface portion in said second external device are formed on the same semiconductor substrate.

13. (Currently Amended) A data processor connected with a device having a PCMCIA interface via a bus, wherein the PCMCIA control information of said device is stored in a TLB provided in said data processor,

wherein the PCMCIA control information is an information which specifies at least one of an access timing, a memory attribute, and a bus width of said device.

14. (Currently Amended) A data processing system comprising:

a data processor connected via a system bus; and

a device having a PCMCIA interface,

wherein said data processor keeps the PCMCIA control information of said device in an address translation buffer provided in said data processor, translates an address necessary to access said device by said address translation buffer at the time of accessing said device, and controls said device in accordance with said control information kept in said address translation buffer,

wherein the PCMCIA control information is an information which specifies at least one of an access timing, a memory attribute, and a bus width of said device.

15. (Currently Amended) A data processor comprising:

a CPU for outputting a first address;

address translation means for inputting said first address, translating said first address to a second address, and outputting said second address; and

address output means for inputting said second address and outputting said second address to an external device having a PCMCIA interface,

wherein said address translation means stores an external device control information for controlling said external device in association with at least either one of said first address or said second address,

when said first address is inputted to said address translation means, said address translation means outputs said external device control information to said address output means based on said first address or said second address translated based on said first address, and

said address output means outputs said external device control information to said external device,

wherein said external device control information is an information which specifies at least one of an access timing, a memory attribute, and a bus width of said device.

16. (Original) A data processor according to claim 15, wherein said external device control information includes an information which specifies at least one of an access timing, a memory attribute, or a bus width of a device having said PCMCIA interface.

17. (Previously Presented) A data processor according to claim 15, wherein said CPU and a PCMCIA interface in said external device are formed on the same semiconductor substrate.

18. (Previously Added) A data processor comprising:

a CPU for outputting a first address;

address translation means for inputting said first address, translating said first address to a second address, and outputting said second address; and

external bus control means for inputting said second address and outputting said second address to an external device,

wherein said address translation means has an address translation buffer, a register, and selection means,

said address translation buffer stores a first external device control information for controlling said external device in association with either said first address

or said second address,

said register has a second external device control information, and

said selection means selects either said first external device control information or said second external device control information and outputs a selected information to said external bus control means.

19. (Previously Added) A data processor according to claim 18, wherein said external device is a device having a PCMCIA interface, and

each of said first external device control information and said second external device control information is an information which specifies at least one of an access timing, a memory attribute, or a bus width of said external device.

20. (Previously Added) A data processor according to claim 18, wherein said first selection means outputs said second external device control information stored in said register to said external bus control means when said address translation buffer is not used.

21. (Previously Added) A data processor according to claim 18, wherein said address translation means further comprises an address decoder for receiving said first address and

said first selection means selects either said first external device control information or said second external device control information based on a result of decoding of said address decoder and outputs a selected information to said external bus control means.

22. (Currently Amended) A data processor comprising:

a CPU for outputting a virtual address;

first address translation means and second address translation means for inputting said virtual address, translating said virtual address to a physical address, and outputting said physical address; and

external bus control means for inputting said physical address and outputting to an external device,

wherein said first and said second address translation means stores an external device control information for controlling said external device in association with either said first address or said second address, and

there is provided selection means for selecting

either said external device control information outputted from said first address translation means or said external device control information outputted from said second address translation means and outputting to said external bus control means,

wherein said external device control information is an information which specifies at least one of an access timing, a memory attribute, and a bus width of said device.

23. (Previously Added) A data processor according to claim 22, wherein said first address translation means has an address translation buffer for instruction and said second address translation means has an address translation buffer for data.

24. (Previously Added) A data processor according to claim 22, wherein said first address translation means has an address translation buffer for instruction and said second address translation means has an address translation buffer.

25. (Previously Added) A data processor according to claim 22, wherein said external device is a device having a PCMCIA interface and

said external device control information is an

information which specifies at least one of an access timing, a memory attribute, or a bus width of said external device.

26. (Previously Presented) A data processor comprising:

a CPU for outputting a first address;

address translation means for inputting said first address, translating said first address to a second address, and outputting said second address; and

address output means for inputting said second address and outputting said second address to an external device,

wherein said address translation means stores an external device control information for controlling said external device in association with at least either one of said first address or said second address and outputs said external device control information to said address output means,

wherein said external device control information is an information which specifies at least one of an access timing, a memory attribute, and a bus width of said device.

27. (Previously Presented) A data processor according to claim 26, wherein said external device is a device having a PCMCIA interface.

28. (Previously Added) A data processor according to claim 27, wherein said address output means comprises a timing controller and a bus width and memory attribute decider.

29. (Previously Added) A data processor according to claims 27, wherein said CPU, said address translation means, said address output means, and a PCMCIA interface in said external device are formed on the same semiconductor substrate.

30. (Previously Added) A data processor according to claim 26, wherein said second address outputted from said address output means is inputted to said address output means via a cache memory and a bus.

31. (Previously Added) A data processor according to claim 26, wherein the control information except for an address is not included in said first address.

32. (Currently Amended) A data processor comprising:

a CPU for outputting a first address;

address translation means for inputting said first address, translating said first address to a second address,

and outputting said second address; and

external bus control means for inputting said second address and outputting said second address to an external device having a PCMCIA interface,

wherein said address translation means stores an external device control information for controlling said external device in association with at least either one of said first address or said second address, and when said first address is inputted to said address translation means, said address translation means outputs said external device control information to said external bus control means based on said first address or said second address translated based on said first address,

wherein said external device control information is an information which specifies at least one of an access timing, a memory attribute, and a bus width of said device.

33. (Previously Added) A data processor according to claim 32, wherein said external device control information is an information which specifies at least one of an access timing, a memory attribute, and a bus width of said external device.

34. (Previously Presented) A data processing system comprising:

a first address for being outputted by a CPU;

address translation means for translating said first address to a second address; and

address output means for outputting an address to a first external device and a second external device,

wherein when said first address is outputted to said first external device via said address output means, said address translation means outputs a first external device control information stored in association with said first address to said address output means, and

when said second address is outputted to said second external device via said address output means, said address translation means outputs a second external device control information stored in association with either said first address or said second address to said address output means,

wherein said external device control information is an information which specifies at least one of an access timing, a memory attribute, and a bus width of said device.

35. (Previously Added) A data processing system according to claim 34, wherein said second external device is a device having a PCMCIA interface.

36. (Canceled).

37. (Previously Added) A data processing system according to claim 34, wherein said address translation means outputs said second address and

said second address is inputted to said address output means via a cache memory and a bus.

38. (Previously Added) A data processing system according to claim 34, wherein said second external device has a memory or a modem, and said memory or said modem are controlled by said PCMCIA interface controlled by said second external device control information.

39. (Previously Added) A data processing system according to claim 34, wherein said CPU, said address translation means, said address output means, and a PCMCIA interface portion in said second external device are formed on the same semiconductor substrate.